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REMARKS

Claims 1- 21 are pending in this application. By this Amendment, Applicants AMEND claim 14.

Applicants greatly appreciate the Examiner's indication that claim 2 would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claim.

The Examiner has indicated that the outstanding Office Action is a Final Office Action because the new ground of rejection was **necessitated** by Applicant's Amendment (see paragraph no. 5 on page 5 of the Office Action).

First, in the Amendment dated August 16, 2002, Applicants amended claims 1, 9, 13, and 14 in response to the Examiner's rejection of claims 1, 9, 13, and 14 under 35 U.S.C. §112, second paragraph in the Office Action, dated May 16, 2002. In the independent claims 1 and 14, Applicants added the phrase "of the chip electronic component" in lines 2 and 5 to modify the term "body." However, **THIS IS NOT A NEW LIMITATION**. The phrase "body of the chip electronic component" was already recited in line 11 of both claims 1 and 14. Further, Applicants' only other amendment was to replace "being included in" with --defining part of--. No new features were added to the claims by the Amendment dated August 16, 2002. Applicants only made a minor clarification.

It is beyond reason to conclude that the minor clarifying amendment of replacing "being included in" with --defining part of-- **necessitated** a new ground of rejection.

Second, in response to the Examiner's prior art rejection of claims 1, 2, 6-12, 14-18, 20 and 21 under 35 U.S.C. § 103(a) as being unpatentable over Gamo (U.S. 6,011,451) in view of Kuroda et al. (U.S. 6,215,229), Applicants filed a Declaration under 37 C.F.R. § 1.130 indicating that the present invention and the inventions described in Gamo and Kuroda et al. were at the time the inventions were made, commonly owned by the same company. That is, **NO** amendments were made in response to the Examiner's prior art rejection.

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The Examiner is reminded that the Examiner should anticipate that a statement averring common ownership at the time the invention was made may disqualify any patent or application applied in a rejection under 35 U.S.C. 103 based on 35 U.S.C. 102(e). See the fourth paragraph of MPEP § 706.07(a). In fact, the Examiner was on notice that the two inventions were commonly owned at the time of invention. First, Masaya Wajima is a common inventor in both Kuroda et al. and the present application. Second, Applicants filed an assignment on September 6, 2000 (the filing date of the present application) indicating the present application was assigned to Murata Manufacturing Co., Ltd which is the same assignee as Gamo and Kuroda et al. The M.P.E.P. has made it quite clear that an Examiner cannot make an Office Action a Final Office Action solely because Applicants have filed a Declaration under 37 C.F.R. § 1.130.

Accordingly, Applicants respectfully request reconsideration and withdrawal of the Finality of the Office Action, dated October 23, 2002.

Claims 1 and 3-21 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Kaida (U.S. 5,684,436) in view of Kaida et al. (U.S. 5,627,425) and Okamura (U.S. 5,892,415). Applicants respectfully traverse the rejection of claims 1 and 3-21.

Claim 1 recites:

"A chip electronic component comprising:
a body of the chip electronic component having outer peripheral surfaces including an upper surface, a lower surface and a pair of side surfaces;
an electronic component element having electrodes and defining part of said body of the chip electronic component; and
a plurality of external electrodes arranged to extend over at least the lower surface and at least one of the side surfaces of said body of the chip electronic component and electrically connected to the electrodes of the electronic component element; wherein
each portion of said external electrodes provided on the lower surface of said body of the chip electronic component is provided with a narrow portion and a wide portion." (emphasis added)

Claim 14 has been amended to recite:

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"14. A chip electronic component comprising:
a body of the chip electronic component having outer peripheral surfaces including an upper surface, a lower surface and a pair of side surfaces;
an electronic component element having electrodes and defining part of said body of the chip electronic component; and
a plurality of external electrodes arranged so as to extend over at least the lower surface and at least one of the side surfaces of said body of the chip electronic component and electrically connected to the electrodes of the electronic component element;
wherein **each portion of said external electrodes provided on the lower surface of said body of the chip electronic component is arranged to have an almost uniform width from one longitudinal end to the other, and satisfy the relation $L_1 < L_3$, where L_3 is the width of each portion of the external electrodes provided on the lower surface of said body of the chip electronic component, and L_1 is the width of each portion of the external electrodes provided on the at least one side surface of said body of the chip electronic component, each of the widths L_1 and L_3 being defined as a dimension of the external electrodes measured in a longitudinal direction of the body of the chip electronic component.**" (emphasis added)

Applicants' claim 1 recites the feature of "each portion of said external electrodes provided on the lower surface of said body of the chip electronic component is provided with a narrow portion and a wide portion." Applicants' claim 14 recites the feature of "wherein each portion of said external electrodes provided on the lower surface of said body of the chip electronic component is arranged to have an almost uniform width from one longitudinal end to the other, and satisfy the relation $L_1 < L_3$, where L_3 is the width of each portion of the external electrodes provided on the lower surface of said body of the chip electronic component, and L_1 is the width of each portion of the external electrodes provided on the at least one side surface of said body of the chip electronic component, each of the widths L_1 and L_3 being defined as a dimension of the external electrodes measured in a longitudinal direction of the body of the chip electronic component."

With the improved features of claims 1 and 14, Applicants have been able to provide a chip electronic component and a mounting structure for the same that is not susceptible to stress caused by warpage of the substrate on which it is mounted,

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thereby ensuring a reliable electrical connection and a strong mechanical bond, and further, simplifying the manufacture of the chip electronic component and mounting structure thereof, without requiring complicated manufacturing processes (see, for example, the paragraph bridging pages 6 and 7 of the Specification).

The Examiner has alleged that Kaida shows in **Figs. 37 and 38** the features of "each portion of said external electrodes provided on the lower surface of said body of the chip electronic component is provided with a narrow portion and a wide portion" as recited in Applicants' claim 1. The Examiner has alleged that reference numbers **33a** and **33d** show these features. However, reference numbers **33a** and **33d** clearly are directed to wide and narrow portions of the internal electrodes of the chip electronic component, NOT to wide and narrow portions of the external electrodes of a chip electronic component as recited in Applicants' claim 1.

The Examiner has relied upon Okamura and Kaida et al. to cure various deficiencies of Kaida. However, neither Okamura nor Kaida et al. teach or suggests the feature of "each portion of said external electrodes provided on the lower surface of said body of the chip electronic component is provided with a narrow portion and a wide portion" as recited in Applicants' claim 1.

Further, it does not appear from paragraph no. 2 of the Office Action that the Examiner relied upon either Okamura or Kaida et al. in his rejection of claim 1. First, the Examiner relied upon Okamura et al. to teach the features of using a printed circuit board and using a conductive bond, neither of which is recited in claim 1. Second, the Examiner relied upon Kaida et al. to teach different widths of the electrodes located on the lower and side surfaces, which is not recited in claim 1.

Accordingly, Applicants respectfully request reconsideration and withdrawal of the rejection of claim 1 under 35 U.S.C. §103(a) as being unpatentable over Kaida in view of Kaida et al. and Okamura.

Applicants agree with the Examiner that Kaida does not teach or suggest the features of "wherein each portion of said external electrodes provided on the lower

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surface of said body of the chip electronic component is arranged to have an almost uniform width from one longitudinal end to the other, and satisfy the relation $L_1 < L_3$, where L_3 is the width of each portion of the external electrodes provided on the lower surface of said body of the chip electronic component, and L_1 is the width of each portion of the external electrodes provided on the at least one side surface of said body of the chip electronic component, each of the widths L_1 and L_3 being defined as a dimension of the external electrodes measured in a longitudinal direction of the body of the chip electronic component" as recited in Applicants' claim 14. The Examiner has relied upon Kaida et al. to teach these features.

First, Kaida et al. shows in **Figs. 38 and 39** the features of the external electrodes on the **upper** surface of the chip electronic component, **NOT** any of the features of the external electrodes on the **lower** surface of the chip electronic as recited in Applicants' claim 14.

Second, Kaida et al. clearly fails to teach or suggest the feature of "wherein each portion of said external electrodes provided on the lower surface of said body of the chip electronic component is arranged to have an almost uniform width from one longitudinal end to the other, and satisfy the relation $L_1 < L_3$, where L_3 is the width of each portion of the external electrodes provided on the lower surface of said body of the chip electronic component, and L_1 is the width of each portion of the external electrodes provided on the at least one side surface of said body of the chip electronic component each of the widths L_1 and L_3 being defined as a dimension of the external electrodes measured in a longitudinal direction of the body of the chip electronic component" as recited in Applicants' claim 14. Applicants have provided a marked-up copy of **Fig. 9** of the present application and **Fig. 39** of Kaida et al. to assist the Examiner in understanding the differences between the present claimed invention and the prior art.

As recited in Applicants' claim 14, the width direction of the portion of the external electrode disposed on the lower surface is measured in the longitudinal direction of the body of the electronic component element. As recited in Applicants' claim 14, the width

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of the portion of the external electrode disposed on the side surface of the body of the chip electronic component is measured in the longitudinal direction of the body of the electronic component element. Using the widths as recited in Applicants' claim 14, Kaida et al. clearly teaches that the width of the portion of the external electrode disposed on the side surface of the body of the electronic component is **exactly the same** as the width of the external electrode disposed on the lower surface of the body of the electronic component, **NOT** that the width of the portion of the external electrode disposed on the bottom surface of the body of the electronic component is **less than** the width of the external electrode disposed on the lower surface of the body of the electronic component.

The Examiner has relied upon Okamura to teach the features of using a printed circuit board and using a conductive bond. However, neither of these features is recited in Applicants' claim 14. Additionally, Okamura clearly fails to teach or suggest "each portion of said external electrodes provided on the lower surface of said body of the chip electronic component is arranged to have an almost uniform width from one longitudinal end to the other, and satisfy the relation $L_1 < L_3$, where L_3 is the width of each portion of the external electrodes provided on the lower surface of said body of the chip electronic component, and L_1 is the width of each portion of the external electrodes provided on the at least one side surface of said body of the chip electronic component each of the widths L_1 and L_3 being defined as a dimension of the external electrodes measured in a longitudinal direction of the body of the chip electronic component" as recited in Applicants' claim 14.

Accordingly, Applicants respectfully request reconsideration and withdrawal of the rejection of claim 14 under 35 U.S.C. §103(a) as being unpatentable over Kaida in view of Kaida et al. and Okamura.

Accordingly, Applicants respectfully submit that Kaida, Kaida et al., and Okamura, applied alone or in combination, fail to teach or suggest the unique combination and arrangement of elements recited in claims 1 and 14 of the present

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application. Claims 3-13 depend upon claim 1, and are therefore allowable for at least the reasons that claim 1 is allowable. Claims 15-21 depend upon claim 14, and are therefore allowable for at least the reasons that claim 14 is allowable.

In view of the foregoing amendments and remarks, Applicants respectfully submit that this application is in condition for allowance. Favorable consideration and prompt allowance are solicited.

To the extent necessary, Applicants petition the Commissioner for a TWO-month extension of time, extending to March 23, 2003, the period for response to the Office Action dated October 23, 2002.

The Commissioner is authorized to charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account No. 50-1353.

Respectfully submitted,

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VERSION WITH MARKINGS SHOWING CHANGES MADE

14. (Twice amended) A chip electronic component comprising:
- a body of the chip electronic component having outer peripheral surfaces including an upper surface, a lower surface and a pair of side surfaces;
 - an electronic component element having electrodes and defining part of said body of the chip electronic component; and
 - a plurality of external electrodes arranged so as to extend over at least the lower surface and at least one of the side surfaces of said body of the chip electronic component and electrically connected to the electrodes of the electronic component element;
- wherein each portion of said external electrodes provided on the lower surface of said body of the chip electronic component is arranged to have an almost uniform width from one longitudinal end to the other, and satisfy the relation $L_1 < L_3$, where L_3 is the width of each portion of the external electrodes provided on the lower surface of said body of the chip electronic component, and L_1 is the width of each portion of the external electrodes provided on the at least one side surface of said body of the chip electronic component, each of the widths L_1 and L_3 being defined as a dimension of the external electrodes measured in a longitudinal direction of the body of the chip electronic component.

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[図9] FIG. 9

width of the
portion of the
external electrode
disposed on the
side surface

width of the
portion of the
external electrode
disposed on the
lower surface

longitudinal
direction of
the body of the
chip electronic component

